Experimental technology and performance of 0.1-μm-gate-length FETs operated at liquid-nitrogen temperature

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An overview is presented of our work to explore the extendibility of the silicon FET technology to the 0.1-μm-gate-length level. Self-aligned, n-channel, polysilicon-gated FETs were designed for operation at 77 K, with reduced power-supply voltage. Direct-write electron-beam lithography was used to pattern all levels, while other processing followed established lines. Noteworthy results of the work included the observation of a clear manifestation of velocity overshoot, which contributed to achieving extrinsic transconductances above 940 μS/μm at 0.07-μm gate length. The measured switching delay of ring oscillators which contained 0.1-μm-gate-length devices was as low as 13.1 ps, with simulations showing potential for reduction to below 5 ps. Both the transconductance and the switching times are the best values observed for FETs to date—indicating continuing value in the scaling of FETs to dimensions well beyond those currently used.

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Introduction

Field-effect transistors (FETs) fabricated from silicon are the most commonly used devices in integrated circuit chips. Their fabrication is relatively simple, the material quality of silicon is superior to that of any other semiconductor, and the power consumption of FETs is relatively low. Consequently, chip integration has reached levels of millions of such devices in chips having an area typically 1–2 cm^2. In those applications requiring the

highest performance, bipolar transistors have long been superior, and III–V compound semiconductors have been investigated as a potential replacement for silicon. However, silicon FETs have a well-established scaling path [1] which leads concomitantly to smaller device dimensions and increased performance. If FETs can stay on track, their performance may eventually exceed that of other devices. Indeed, the past two decades have seen the continued progress of FET technology along the indicated scaling path.

Whether the miniaturization of silicon FETs is approaching an end has been a subject of long-standing interest. In the deeply submicrometer regime, classical FET scaling [1] runs into a variety of nonscaling parameters and associated detrimental effects. Among others, these include mobility degradation [2], inversion-layer broadening [3], tunneling through the gate insulator, and the onset of velocity saturation. These effects are worsened by the fact that the operating voltage cannot be scaled along with dimensions past a level where the nonscaling turn-off behavior of FETs becomes significant. However, cooling to low temperatures reduces that problem. Continuing miniaturization and the use of low voltages may also lead to advantages, such as the possibility of velocity overshoot in very short devices [4] and the weakening of those detrimental effects that are associated with an energy threshold. For instance, regardless of what magnitude the electric field may reach, carriers with sufficient energy to create an electron–hole pair and cause avalanching become scarce when the operating voltage decreases below the bandgap value. Apart from fundamental physical effects, the practical return from shrinking dimensions hinges on overcoming difficulties such as linewidth and alignment control, thin insulator reliability, shallow junction fabrication, the limitations of contact and spreading resistivities, and many other considerations. Although there have been many theoretical treatments of the perceived limits of silicon FET technology, prior to our efforts relatively little experimental work [5–8] had been performed in the deeply submicron regime.

Several considerations motivated the work described in this paper. There was a desire to understand the limits of mainline-scaled FETs and to ascertain how far established notions of FET behavior and classical transport would remain valid along the scaling path. We wanted to discover what, if any, new effects would be encountered. From a practical point of view, it was important to explore the extendability of the FET technology, and determine what performance could be expected. To address these matters, an investigation of 0.1-μm-gate-length FET behavior was considered to be a sufficiently significant step and within the reach of our capabilities. We decided to carry out these studies primarily at liquid-nitrogen temperature because of the fundamental superiority of low-temperature operation. In addition to offering device design advantages, low-temperature operation is a key to overcoming the resistance problem in interconnection line scaling [9].

Design and test structures

Operating voltage cannot be indefinitely decreased with dimensions because of nonscalable parameters and noise margins. As a result, one is forced to work with higher voltage levels than are dictated by ideal scaling. This becomes most detrimental once performance saturates at less than the specified operating voltage due to velocity saturation-type characteristics. In such an environment, the use of higher voltage leads only to increased power consumption without an accompanying increase in performance. Thus, the measure of a good design lies in achieving operation at the lowest feasible voltage. That requirement inevitably leads to a low-temperature (LT), 77 K, design. Operation at LT reduces the minimum allowable FET threshold voltage by increasing the turn-off rate below threshold, and by reducing threshold voltage changes caused by temperature variations. Since these two effects are the main obstacles to lowering the threshold, and thus the operating voltage, LT affords a design point which is not reachable at room temperature (RT). LT operation entails further advantages [10], including improved performance, lower interconnection line resistance, and better punch-through behavior. It is not clear whether a worthwhile RT design can be found for 0.1-μm-gate-length FETs.

As a first feasibility study at the 0.1-μm-gate-length level, our efforts were directed exclusively toward n-channel devices (NMOS). In accordance with classical scaling, the general design approach was to reduce all horizontal and vertical dimensions, as well as operating voltages, proportionately with gate length. However, ideal scaling had to be modified in some instances. Due to noise margins, subthreshold turn-off, and threshold sensitivity arising from process variations, the lowest threshold voltage considered to be practical even at LT was 150 mV, the same level which had been proposed for a 0.25-μm LT design [11]. This design point leads to the use of a 0.6–0.8-V power supply (V_{dd}). With the exception of the gate oxide, all vertical dimensions were scaled commensurately with the 0.1-μm-gate-length design. For reliability reasons the gate oxide was grown to 4.5 nm in most cases, rather than the ~2.5-nm value called for by full scaling. In the horizontal direction, the source/drain and isolation dimensions were not fully scaled. Since full scaling of this level was not regarded as critical for the main purposes of the work, by implementing the relatively relaxed 0.25-μm ground rules we could make use of a simple semi-recessed oxide isolation.

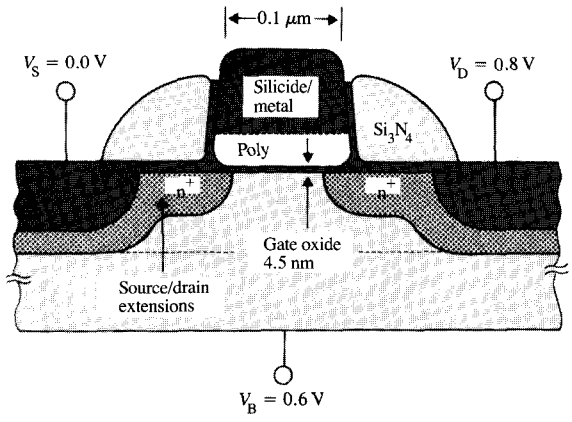

Figure 1

Schematic of device cross section and bias levels. (From [5], reproduced with permission; © 1987 IEEE.)

In order to reduce geometry effects in short-channel devices, it is necessary to reduce depletion layer widths. In scaling, this is accomplished by increasing the substrate doping and lowering the applied voltage. However, for these very small FETs the built-in junction potential becomes significant in comparison to the applied voltage, particularly at 77 K. This can be counteracted by forward-biasing the substrate, which can be tolerated at LT without undue increase in the leakage current. A 0.6-V forward bias [11] was employed. The doping levels were chosen to be consistent with the design of the 0.1-μm-gate-length devices (for brevity, 0.1-μm devices), resulting in appropriate threshold, substrate sensitivity, and punch-through control for that gate length.

The basic device chosen for our investigations was of a source/drain-extension-type structure [12]. A schematic cross section of the device, with design voltage levels indicated, is shown in **Figure 1**. This structure provides shallow junctions near the gate, and deeper junctions displaced from the gate by a spacer, allowing for formation of self-aligned metal on the diffusions. Much attention was paid to ensure low source/drain (S/D) resistance. This was important because use of gate oxides thinner than 5 nm could result in an extremely high intrinsic transconductance, thus causing the S/D resistance to become the single most important factor in determining the extrinsic transconductance. To achieve a very low S/D resistance, antimony was used in some of the S/D extensions, since for very shallow junctions antimony had advantages over arsenic [13]. To minimize the impact of impurity scattering on inversion-layer carrier mobility at 77 K, the doping in the channel was peaked away from the surface. The ion-implantation energies which were used were chosen to provide the lowest possible sensitivity to process variations.

Since the electron-beam lithography system used for patterning placed limitations on the size of a given chip, seven different test chip designs were assembled with a variety of structures. Three of the chip designs contained ring oscillators and inverter chains; the others contained various parametric test sites. Simple circuits were also included to measure the capacitances of the small gates during device operation, to observe gate leakage, and to measure intrinsic transconductance and device noise. Many of the test structures were used previously in our laboratory in their larger versions [12]. Most of the structures were replicated with different gate lengths at the design level, ranging from over 0.25 μm to less than 0.1 μm, with several gate widths ranging from 0.5 μm to 11 μm. The small devices were complemented by large ones, 100 μm in length and 50 μm in width. **Figure 2** shows a micrograph of an illustrative chip.

Fabrication

Details of the lithographic processes which were used may be found in References [6] and [14]. Briefly, five lithographic levels, including one for alignment marks, were all performed in a Gaussian electron-beam system, with a high-resolution field size of 250 μm × 250 μm. The system was designed specifically for below-0.1-μm lithography with a minimum probe size of 8 nm. It could be operated at up to 80 kV, with 25 kV being the typical value used for this work. Electronic noise, vibrations, and other interferences were carefully reduced to a level which was consistent with the nanometer lithography requirements.

The highest-resolution step was associated with gate fabrication. It was performed by lift-off of a metal stencil using double-layer PMMA, followed by reactive ion etching (RIE) to form the polysilicon gates down to 70 nm in minimum dimension. Lithography for the contact holes, for which resolution below 0.2 μm was required, was achieved using a Novolac-based resist. This resist exhibited excellent behavior during contact hole opening, which involved oxide RIE. The level-to-level overlay was found to be consistently better than 30 nm. This was achieved using tantalum silicide alignment marks with 0.25-μm minimum features and fourfold redundancy, lifted off at the first lithography level. The high-resolution alignment capability facilitated the layout of devices and circuits that had minimal parasitic effects.

The fabrication was carried to completion on eight wafers. With the exception of the lithography steps, all processing was done in the clean-room facilities of our laboratory. To study the sensitivities and extendibility of the processes used, many experimental variations were

introduced. In the end, no two wafers had received exactly the same processing. On all the wafers but two, 4.5-nm-thick gate oxide was grown. One contained a 3.3-nm-thick gate oxide, and another contained a very thick one for special measurements. The oxide thicknesses were measured during processing by ellipsometry, and by capacitance upon completion. The main process steps used, some of the reasons behind them, and the significant experimental variations are outlined below in an abbreviated form:

1. Implant boron into the back side of 2-Ω-cm p-type substrates to provide good contact at 77 K.
2. Lift off $TaSi_2$ alignment marks, containing minimum dimensions of 0.25 μm.
3. Grow 10 nm pad oxide and deposit 100 nm nitride. Pattern the diffusion regions. Implant channel stop boron. Grow 160 nm dry, semi-recessed field oxide at 950°C.
4. Strip the nitride–oxide stack from diffusion regions. Implant boron for threshold control and punch-through stop. Doses ranged from 2.5 to 5.5 $\times 10^{12}/cm^2$. In most cases two implant energies, 15 and 30 keV, were used.
5. Grow thermal SiO_2 gate insulator at 800°C in dry oxygen with HCl.
6. Deposit 100-nm-thick undoped polysilicon from which to form the gates.
7. Write gate pattern in a double-layer PMMA resist. Lift off metal using this pattern to form an etch mask. Etch gates using a two-step RIE process.
8. Grow 7.5 nm oxide on polysilicon at 850°C in dry oxygen with HCl.
9. Implant S/D extensions [12]. Both arsenic and antimony were utilized as dopant species. Doses were in the few times $10^{14}/cm^2$ range, with energy down to 10 keV. Multiple-energy implants were used in some cases to achieve a more "boxlike" profile.
10. Deposit and reactive-ion-etch 100 nm nitride to form an insulating gate-sidewall spacer.
11. Implant arsenic S/D and gates. Doses were 2 to 5 $\times 10^{15}/cm^2$, at 20 keV.
12. Activate S/D. Furnace thermal budgets ranged from 850°C, 20 minutes to 900°C, 30 minutes. Some wafers received rapid thermal anneals of 1050°C and 1100°C for 10 s. The final depth was estimated to be ~50 nm for the S/D extensions and 100 nm for the "deep" junctions.
13. Form self-aligned titanium silicide ($TiSi_2$) on selected wafers.
14. Deposit 100 nm low-temperature conformal oxide overlay.
15. Pattern contact hole level, and reactive-ion-etch contact openings.

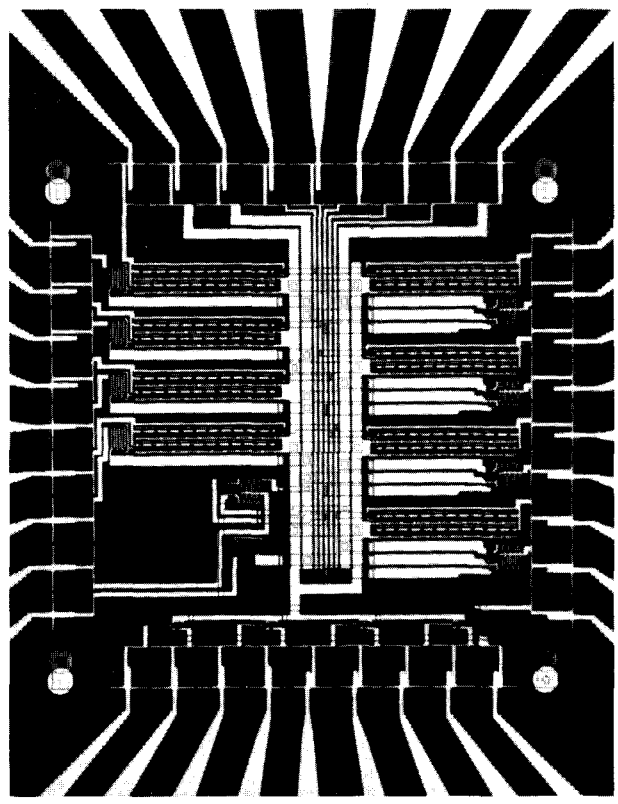

Figure 2

Micrograph of illustrative chip, containing ring oscillators. Individual inverter stages are visible at the bottom of the chip.

16. Form metal level by lift-off of 300 nm of Ti/Al and anneal in a partial hydrogen ambient.

Figures 3 and **4** illustrate the precision in the fabrication process. An SEM micrograph of an inverter stage of a ring oscillator is shown in Figure 3. To observe the smallest features it is necessary to remove the metal and the interelectrode oxide. Figure 4 shows an SEM micrograph of an inverter containing 0.07-μm-long gates, following the removal of its upper layers.

Self-aligned silicidation turned out to be the processing step which was most difficult to execute with satisfactory results. Standard heat treatments in the 800°C and 30 minutes range caused gate shorts to the S/D and/or the channel. Although the silicidation consumed only a fraction of the polysilicon thickness, in certain spots the Ti diffused along grain boundaries much beyond the average depth. Once the Ti came into contact with the gate oxide, the devices were ruined. The problem was solved by resorting to rapid thermal processing using annealing times of 10 to 30 s. However, the sheet resistivity of the final $TiSi_2$ was not satisfactory, being

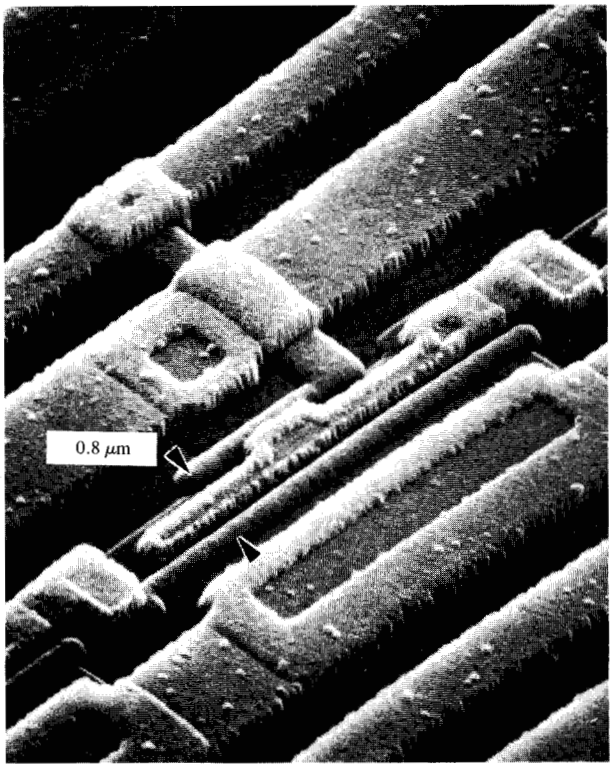

Figure 3

SEM micrograph of an inverter stage of a ring oscillator.

typically in the 30-Ω/□ range, instead of <10 Ω/□. Furthermore, it was discovered that for the thinnest silicided lines the specific sheet resistance increased with respect to the values obtained on lines from 2 to 0.25 μm. On the 0.1-μm-wide lines this increase was ~30%. The effect was probably due to the fact that when the grain size of the $TiSi_2$ became comparable to the line width, the current flow in that material became hindered, and finally was forced to enter, at an increasing rate, the much-higher-resistivity polysilicon. An initial solution for this problem might be the use of thicker polysilicon. Longer-range solutions might include, for instance, schemes that would not involve the self-aligned silicidation of gate and S/D. The main contribution to the overall S/D resistance, as is discussed later, does not come from the resistivity of the deep part of the S/D, which is the one that benefits the most from use of the self-aligned scheme. While the silicide resistivity problem is not deemed to be insurmountable, in the present work it did detrimentally affect circuit performance.

Characteristics and performance

Approximately 75% of all of the tested structures were operational. This percentage included some sites that depended on the operation of many devices, such as inverter chains and ring oscillators. Quite a few of the structures, however, had higher than expected junction or gate leakage. These leakages occurred in a random fashion, independently of gate length. Overall, the yield could be considered quite satisfactory, considering the experimental nature of the work, which entailed no unusual provisions for contamination control.

Not surprisingly, no "generic" 0.1-μm device behavior was found. Extrinsic characteristics strongly depended on the processing variations introduced during fabrication, the reason simply being that 0.1-μm device behavior can be dominated by parasitic contributions. Thus, careful fabrication with focus on minimizing the most important parasitics was critical in achieving high-performance devices. Comparisons of device behavior as a function of processing have been presented earlier [5, 15]. Here we place more emphasis on the more fundamental aspects of our investigations.

We first show results which are important from a device design point of view. **Figure 5** gives the measured change in threshold voltage as a function of gate length

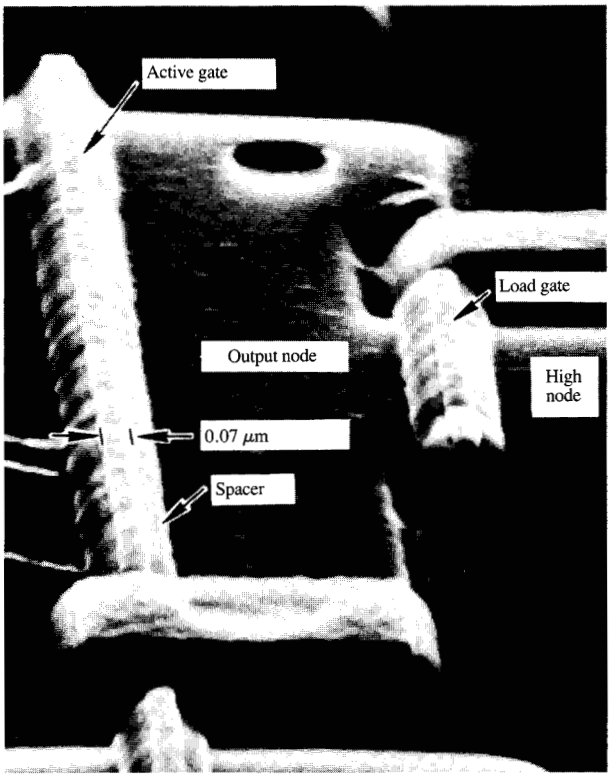

Figure 4

SEM micrograph of an inverter after removing metal, interelectrode oxide, and semi-recessed isolation oxide. (From [5], reproduced with permission; © 1987 IEEE.)

for devices on a given wafer. Throughout this study, gate lengths were measured by SEM. Similar behavior is seen at both room and low temperatures, but the utility of a forward-bias substrate in reducing geometry effects is clearly seen. This characteristic also shows the benefit of the relatively thin gate oxide and the increased channel doping in controlling geometry effects. Because of the enhanced doping concentration provided by the deep channel implant, little punch-through behavior is seen at LT even for the shortest devices. However, the threshold fall-off in Figure 5 at the 0.1-μm gate length would pose very severe requirements on linewidth tolerances, if large numbers of such devices were to be fabricated. On the other hand, the threshold fall-off can be further minimized in several ways. First, oxide thickness could be reduced from the 4.5-nm value. Furthermore, the dose of the deep punch-through control implant could be increased, although this would also increase substrate sensitivity. Finally, a threshold somewhat higher than the proposed nominal 150 mV may be acceptable, since, as is seen later, device performance is quite good even at applied voltages above 1 V. The higher threshold would ease requirements on linewidth tolerances by allowing a wider subthreshold voltage range for minimal devices. In the future, slightly differing designs might be considered, striking an optimum balance between geometry and substrate sensitivity effects, depending on the type of circuits under consideration. **Figure 6** gives the subthreshold slope as a function of gate length measured at RT and LT, showing results in line with expectations.

In order to present as clearly as possible the fundamental aspects of the observed device and circuit behavior, the results given below are from the same single wafer unless indicated otherwise. In this manner, fundamental properties, e.g., correlation of characteristics with gate length, can be isolated from incidental ones, which are mainly due to processing details. The particular wafer chosen for this purpose contained a 4.5-nm-thick gate oxide, antimony S/D extensions, and self-aligned $TiSi_2$ on the S/D and gate. Devices on the wafer had received a single threshold adjust implantation of $5.5 \times 10^{12}/cm^2$ boron at 30 keV energy. The resulting threshold, 0.3 V for the 0.1-μm devices with 0.6 V substrate bias, was at the high end of the range we explored. Although the higher-than-nominal threshold resulted in some disadvantages, this wafer was chosen as representative because it contained the best combination of low S/D resistance and good-quality $TiSi_2$.

We now proceed by first presenting device behavior, and then considering circuit performance.

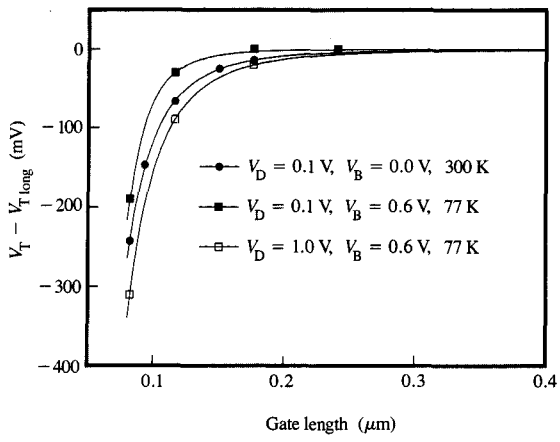

Figure 5

Threshold voltage change as a function of gate length. (From [15], reproduced with permission; © 1987 IEEE.)

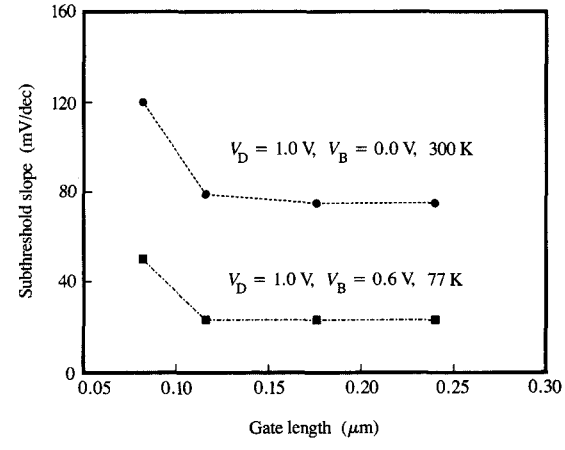

Figure 6

Subthreshold slope as a function of gate length. (From [15], reproduced with permission; © 1987 IEEE.)

• *Device performance and velocity overshoot*

In the subsequent discussions all parameters, unless explicitly specified as "intrinsic," are to be understood as measured values on device terminals. For instance, given transconductances are the measured values without adjustment for parasitic effects. Also, unless RT is specifically indicated, all data and discussion refer to operation at LT.

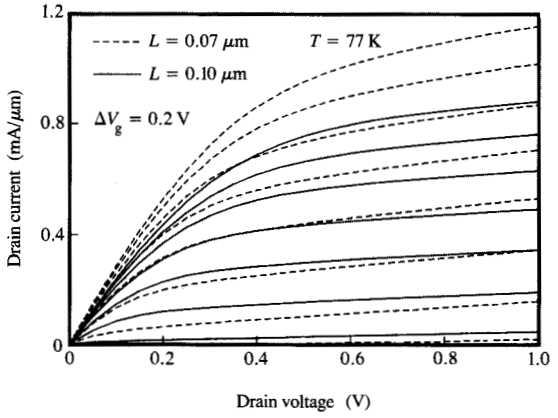

Figure 7

Device terminal characteristics at 77 K. Maximum V_G was 1.5 V and substrate was biased to 0.6 V. The 0.07-μm device at $V_D = 1$ V had a maximum g_m of over 940 μS/μm, while the 0.1-μm device had a maximum g_m of 770 μS/μm. (From [7], reproduced with permission; © 1988 IEEE.)

Figure 7 shows the LT terminal characteristics of the 0.07-μm and 0.1-μm-gate-length devices. As can be seen, the device characteristics were excellent. The 0.07-μm device at 1 V drain voltage, V_d, had a maximum transconductance (g_m) of over 940 μS/μm, while the 0.1-μm one had a maximum transconductance of 770 μS/μm. The room temperature g_m of these devices with 0 V substrate bias was 590 and 505 μS/μm, respectively. Both the LT and RT transconductances were the highest ones measured in silicon FETs, and compared favorably even with values attained with compound semiconductor devices [16]. The same very high transconductances were also measured on another one of our wafers [5, 15]. The common processing feature of the two wafers with the highest transconductances was the antimony S/D extension. The sharp lateral S/D junction edge achieved with antimony was necessary for lowering the parasitic resistances. Detailed device behavior at RT and at longer gate lengths is not discussed here, but has been described in previous publications [5, 6, 15].

It is instructive to assess the performance of such devices in a dense digital circuit environment where wiring capacitances have to be driven over full voltage-signal swings. It can be seen from Figure 7, or from device characteristics presented previously [5, 15], that a ~2.5-μm-wide 0.1-μm-gate-length device, with an input capacitance below 3 fF, can switch over 0.5 mA of current upon a 0.5-V input swing. Such current and voltage values are typical of the highest-performance emitter-coupled-logic (ECL) bipolar circuits. This indicates that the LT 0.1-μm NMOS devices are in a performance domain previously reserved only for bipolar transistors. Such a performance in small FETs is to some extent due to velocity overshoot, the topic to which we next turn our attention.

Velocity overshoot is an effect that can only be observed in devices that are small enough for very strong field gradients to be tolerated over major portions of the device. First predicted by Monte Carlo methods [4], velocity overshoot with simplifications can be derived analytically [17]. However, since the physical picture is sometimes obscured by the formalism, it is worthwhile discussing velocity overshoot in a qualitative manner.

In order to picture velocity overshoot clearly, it is first necessary to consider how velocity saturation arises under steady state conditions. (The term "steady state" is used as a shorthand expression for conditions under which carriers are exposed to only slowly varying fields on both the spatial and temporal scales.) In a steady state situation, there is a one-to-one relationship between the strength of an applied electric field and the average carrier energy. If the field is strong, the carrier energy (E) can be significant, and carriers in such fields are customarily referred to as "hot" carriers. For instance, in a 10^5-V/cm field, electrons in silicon reach an average energy of about 0.8 eV. Due to the one-to-one relationship between carrier energy and field strength (F), the E dependence of the mobility, $\mu(E)$, can be expressed as a dependence on field strength: $\mu(E) \sim \mu(F)$. Hence, one obtains the usual expression for drift velocity: $v_d = \mu(F) \times F$. Velocity saturation comes about because the scattering rate of the carriers increases with energy, and stronger fields lead to higher carrier energy. Ultimately, $\mu(F)$ becomes proportional to $1/F$, and v_d remains constant despite further increases in field strength.

The phenomenon of velocity overshoot arises when either the spatial or the temporal scale (in practice both, because one entails the other) is such that the one-to-one correspondence between the field strength and the average carrier energy breaks down. When carriers experience an abrupt field increase, say from F_1 to F_2, then for a short period before they gain the energy which is the one corresponding to F_2, they can exceed, or overshoot, the velocity that they would reach in steady state under the influence of F_2. To take a specific example, assume that the above-mentioned 10^5-V/cm field were to be applied over a 0.5-μm distance with carriers starting out "cold." A typical electron would gain only a maximum of 0.5 eV, which corresponds to the applied potential. This is barely over half the energy that the carriers would reach in the 10^5-V/cm field under steady state conditions. Consequently, their drift velocity could be much enhanced over its steady state value

because the carriers experience a field strength which, in time, would raise them to 0.8 eV, but the maximum scattering they experience is only as severe as the one they would encounter in a much weaker field, namely the one that in steady state would increase their energy to 0.5 eV.

It is important to understand, however, that carriers under velocity overshoot conditions do not reach the drift velocity based on their zero field mobility: $\mu(0) \times F$; they are only exceeding $\mu(F) \times F$. [Carrier velocities exceeding $\mu(0) \times F$ could occur for ballistic transport.] The various scattering processes available to the carriers in real materials is large, and most depend not only on energy but on momentum as well. To move significantly beyond the simple picture given above, one typically must marshal an array of powerful tools in band-structure theory and Monte Carlo techniques [18, 19].

There are other topics of interest, not related to velocity overshoot, but having commonality with it in that field strength is not the relevant parameter, once absolute voltage levels decrease sufficiently. Foremost in this category is impact ionization. As alluded to in the Introduction, once the applied voltages decrease below the bandgap value, regardless of what magnitude fields reach, only carriers in the high-energy tail of the distribution have sufficient energy to directly create an electron–hole pair. One can, however, envision more "exotic" processes which would result in pair production due to a combined presence of high fields and carriers with energy in the vicinity of the bandgap. For instance, a hot carrier might stimulate band-to-band tunneling by imparting its energy to the tunneling electron. An analogous process, for the case of pair creation by photons in strong electric fields, is the well-known Franz–Keldysh effect. To our knowledge, pair creation by hot-electron-stimulated tunneling has not been quantified to date, but one would expect such processes to have low probability. The net result is that despite strong electric fields in small devices, impact ionization, and in general, hot-electron effects, should not play significant roles, due to the decreased applied voltages. This is the reason we could strive for the sharpest possible S/D junction edges with the use of antimony, and still not expect excessive hot-electron problems.

The drift times and spatial scales in silicon NMOS devices are such that in the deeply submicron regime the effects of velocity overshoot should be observable. Indeed, manifestation of velocity overshoot in the intrinsic behavior of short silicon inversion layers has been reported previously [20, 21]. However, in these investigations S/D resistance dominated terminal characteristics, hiding to a large extent the intrinsic behavior. Overall, however, our results are in qualitative agreement with these previous reports.

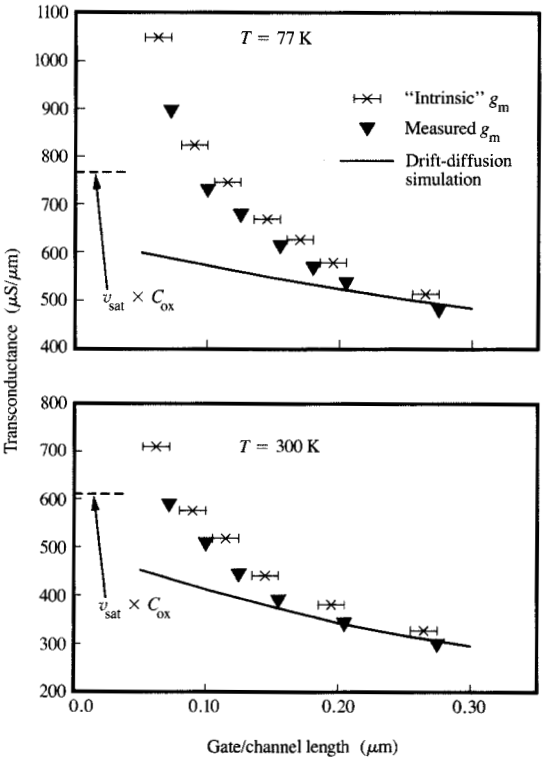

Figure 8

Measured and calculated transconductance at two temperatures. The measured transconductance is plotted versus gate length. The "intrinsic" values are given versus channel length. The solid lines show results of two-dimensional finite element drift-diffusion transport simulations. Limits on the intrinsic transconductance are indicated as $v_{sat} \times C_{ox}$. (From [7], reproduced with permission; © 1988 IEEE.)

Figure 8 shows the transconductance as a function of gate length, and intrinsic g_m as a function of channel length. We define channel length as the distance under the gate between the metallurgical junction edges of the source and drain. The figure shows clear manifestation of velocity overshoot. Two plots were drawn for $V_d = 0.8$ V, and for each gate length at the gate voltage (V_g) at which the transconductance peaked. This typically occurred at the gate drive ($V_g - V_t$), of ~0.6 V, where V_t is the threshold voltage. The transconductances are plotted without fitting or adjustment except for width normalization. On the other hand, the "intrinsic" transconductances and the channel lengths against which they are plotted are the results of fitting, and do contain uncertainties.

The evidence for velocity overshoot is twofold. First, there is the sheer size of the transconductance in the shortest devices. If carriers were not capable of exceeding a saturation velocity (v_{sat}), then there would exist an unattainable upper limit for the intrinsic transconductance, namely: $v_{sat} \times C_{ox}$, with C_{ox} being the oxide capacitance per unit area. This limit is indicated on Figure 8, and as can be seen, even the measured, extrinsic transconductance exceeds it. The second manifestation of velocity overshoot is in the trend of the transconductance with respect to the gate or channel length. However, before dwelling on this point, it is useful to discuss the "intrinsic" properties because that affords an insight into the behavior of deeply submicron devices.

Extensive use was made of a two-dimensional finite element simulator (FIELDAY) [22]. Simulations showed that the details of the S/D lateral junction edge and the extent of the gate overlap of this region were very important in determining transconductance. In the simulations, the lateral S/D junction was assumed to have a several orders of magnitude drop of dopant concentration over 20 nm, since the real antimony junctions have approximately this profile [13]. Despite the abrupt junctions, the short devices behaved like lightly doped drain (LDD) devices. The S/D resistance was strongly dependent on V_g [23], and at large V_d there was a higher voltage drop at the drain edge than at the source edge. Such behavior should not be surprising, once it is realized that a 20-nm junction edge is significant if the channel is as short as 50 to 100 nm. The net result is that the customary treatment of adjusting the transconductance with a single S/D resistance to obtain the intrinsic value is an increasingly poor approximation as gate lengths shrink. Accordingly, the quotes around "intrinsic" in Figure 8 and in the text are intended to indicate the approximate validity of the term.

The difficulty of accurately determining series resistance and channel length in LDD-like devices with strong two-dimensional effects has been recognized previously [24]. This problem was compounded here by uncertainties regarding carrier transport in short channels. For example, at LT, velocity saturation affected the characteristics of the shortest devices even at quite low V_d. The saturation value of the velocity, v_{sat}, was not known with sufficient accuracy in the channel. Additionally, and unexpectedly, the gate drive dependence of the mobility appeared to vary with channel length, particularly at low gate bias. Because of these complications, there remained some uncertainty regarding the channel length. This uncertainty is reflected in the horizontal error bars in Figure 8, where for the "intrinsic" values the abscissa represents channel length. The extracted value of the parasitic S/D resistance was found to be less sensitive to the details of transport than the channel length. The resistances used to calculate the "intrinsic" transconductances of Figure 8 were values averaged over gate drive at low V_d. At LT the total, source plus drain, resistance was found to be between 250 and 270 Ω-μm. The two-dimensional simulations showed that close to 200 Ω-μm of this was due to the S/D edges. The extracted RT value was ~440 Ω-μm. The large difference between the RT and LT resistance was in part due to our test sites, where thin metal lines were leading to large-width-to-length-ratio devices. At LT the metal resistance dropped sufficiently to have only a minor influence on the measurements. Without the contribution from the metal lines, the S/D resistance at RT would have been ~20% higher than that at LT.

A few additional remarks are needed regarding intrinsic behavior and device parameter extraction. The literature abounds with publications proposing various methods for determining intrinsic and extrinsic device parameters. The problem faced with devices as short as the ones we were dealing with is not that a set of parameters cannot be found with which the data can be fitted reasonably well. The problem is that a somewhat different set of parameters fits just as well. There are simply too many degrees of freedom. We see no way out of this problem until a large enough number of samples can be examined to obtain statistically meaningful fits. However, aside from the fitting methods there is a deeper problem as well. Namely, what part of a device can be regarded as truly intrinsic? Even a strict definition of the intrinsic region as being that part of the device which is between the metallurgical junction edges of the S/D is not fully satisfactory. The intrinsic behavior, by definition, should not be affected by external properties. For the shortest devices this is not the case. If one investigates the transport in detail [18, 19, 25], it is clear that the structure of the S/D, its doping level, the doping gradients, the extent of S/D and gate overlap, all feed back to the supposedly intrinsic behavior. This is not to say that these effects are of such magnitude that, for instance, empirical models good enough for circuit simulation could not be obtained. We are only pointing out that one cannot take into account all the details of transport and still maintain the simple picture of an idealized intrinsic device.

We now return to the discussion of velocity overshoot. The solid lines in Figure 8 are the transconductances obtained by using FIELDAY, a sophisticated simulator which handles local, drift-diffusion transport. Since FIELDAY does not treat velocity overshoot, it serves as a gauge to indicate deviations from standard behavior. The simulation was carried out at $(V_g - V_T) = 0.6$ V, $V_d = 0.8$ V, and 0 V substrate bias, the same values for which the data were plotted. A proper amount of external resistance was added to equate it with the ~260 Ω-μm measured

values. The mobilities belonging to $(V_g - V_T) = 0.6$ V gate bias and the saturation velocities which were used in the simulation were 720 cm^2/V-s and 1.0×10^7 cm/s at LT, and 390 cm^2/V-s and 8.0×10^6 cm/s at RT. These values had approximately the same uncertainty as the channel length, having been obtained within the same framework. In the literature v_{sat} values differ significantly [26, 27], with our modeled saturation velocities being close to the high end. The solid curve thus shows how the transconductance would have behaved in the absence of velocity overshoot, and indeed, the transconductance of the longer-gate devices was matched quite well. But the drastic divergence of the modeled curve from the data could only mean that the electron velocity exceeds v_{sat} as the gates become shorter. This is the exact signature expected from velocity overshoot [4, 17].

As alluded to earlier, in the overshoot regime a nonlocal approach to transport is necessary. **Figure 9** shows the velocity obtained from a nonlocal, self-consistent Monte Carlo simulation [18, 19, 25]. According to this modeling, the carriers reach speeds that are more than double that of v_{sat}.

Having established velocity overshoot in the devices, the question is how this will affect circuit behavior. Unfortunately, increased output conductance is an inevitable consequence of velocity overshoot. This is simply due to the fact that at higher drain voltage the relevant carrier velocity is higher, which results in more current. But in most applications higher output conductance is a small price to pay for increased transconductance, the latter being the most important parameter in determining the performance in dense circuits. As indicated in the Introduction, the conventional outlook for miniaturization in the deeply submicron regime is one of diminishing performance returns. However, at really small dimensions, velocity overshoot can increasingly counteract this trend. As such, it provides an additional incentive to continue on the path of miniaturization.

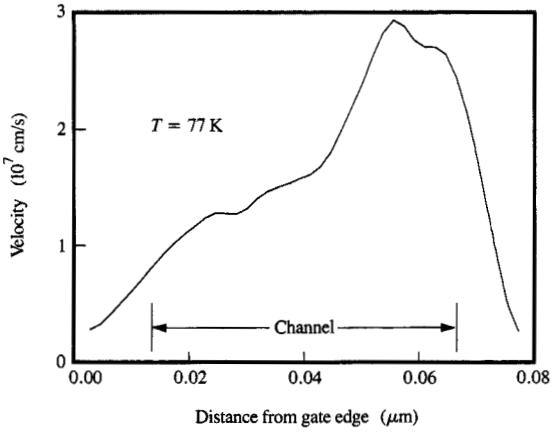

Figure 9

Carrier drift velocity obtained from a two-dimensional self-consistent Monte Carlo simulation for the 0.07-μm device. Biases were assumed to be $V_D = 0.6$ V, $V_G = 0.8$ V, 0 V on substrate. (Courtesy of S. E. Laux and M. V. Fischetti, IBM Thomas J. Watson Research Center.)

• *Circuit performance*

To measure delay times, open-ended inverter chains and unloaded ring oscillators containing 21 stages were fabricated. An enhancement-mode device, with its gate tied to an independent power supply, served as the pull-up element. For the type of device behavior observed at these dimensions, namely roughly constant transconductance in the saturation region, the load device acted as a resistor. The width of the active devices was 5 μm, that of the load devices 1.25 μm. The output of each ring oscillator was buffered into either a push-pull circuit or a source-follower for driving off-chip. The gate length in these support circuits was 0.25 μm. The inverter chains contained the same dimensions and layout as the ring oscillators, but instead of forming a ring they contained one input and two output points. Following a trigger pulse, the difference in the pulse arrival times could be measured at the two outputs. This time difference divided by the number of stages between the outputs, 12 or 8 in our case, gave the delay per stage. The use of redundancy in designing and fabricating ring oscillators and open-ended inverter chains served two purposes. First, the capability to cross-check results obtained from the two different circuit configurations was deemed useful. Second, it ensured the obtaining of a sufficient number of functioning circuits. Successful operation of almost fully scaled circuits on the 0.1-μm scale was not ensured. Although these were quite simple circuits, nonetheless they were the first ones fabricated at that scale.

Ring oscillator and inverter chain operation was tested on 33 chips from five different wafers. Overall, ~70% operation was found, and functionality did not correlate with gate length. For reasons discussed earlier, the results described next were obtained from ring oscillators located on the same wafer which contained the devices discussed in the previous section.

An oscilloscope trace of the output of a ring oscillator containing 0.1-μm devices is shown in **Figure 10**. The delay per stage was 13.1 ps. This is the shortest switching time obtained to date for any type of silicon device at either RT or 77 K [28], including bipolar devices [29].

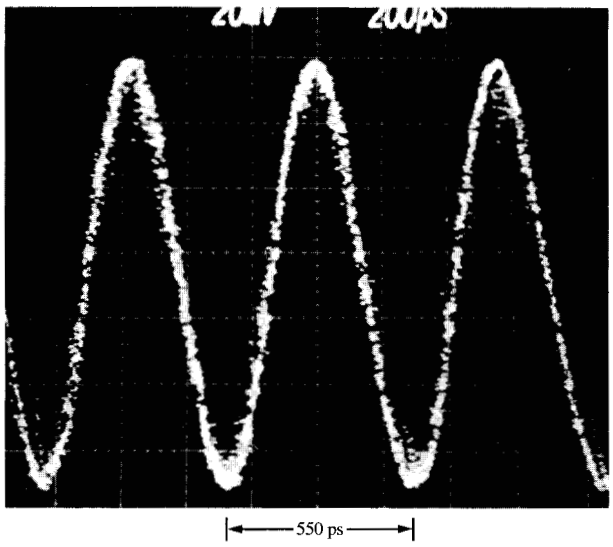

Figure 10

Oscilloscope trace of the output of a 21-stage ring oscillator containing 0.1-μm devices. T = 77 K, V_D = 1.7 V, 0.6 V on substrate. Delay per stage was 13.1 ps. (From [8], reproduced with permission; © 1988 IEEE.)

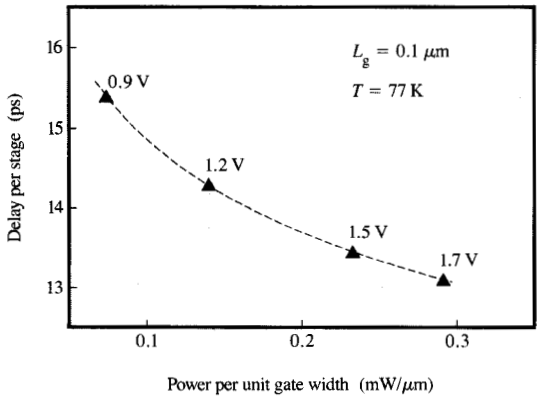

Figure 11

Delay per stage versus power per unit gate width for ring oscillators containing 0.1-μm devices, at 77 K. Power-supply voltage is indicated for each measured point. (From [8], reproduced with permission; © 1988 IEEE.)

The amplitude does not show the internal signal of the ring oscillator; it is only the output of the on-chip driver into a low-impedance load. The swing of the driver was limited by the fact that its power was supplied through a long silicided polysilicon line, which had quite a high resistance. The consistency of all the delay measurements, as well as the excellent characteristics of the individual inverter stages, indicated that the ring oscillators internally underwent a full voltage swing.

Figure 11 shows the switching time versus power. At each applied power-supply voltage the load current was adjusted to obtain the highest speed. As can be seen, the variation is quite flat. A power increase of over a factor of 4 resulted in only 15% delay improvement. This is expected since the devices exhibit transconductance saturation over most of their operational range. The power–delay product at V_{dd} = 0.9 V was 1.1 fJ per 1 μm of channel width. (As a reminder, a 1-μm-wide device in this technology has a width-to-length ratio of 10 to 1.) Had the threshold of these devices been at its nominal design value of 0.15 V, nearly maximum performance might have been attained at the optimal V_{dd} level of 0.6–0.8 V, yielding an even better power–delay product.

The fastest per-stage switching delays measured at selected gate lengths, always on the same wafer, were as follows [8]: 19.5 ps at 0.20 μm, 17.8 ps at 0.16 μm, 16 ps at 0.13 μm, and 13.1 ps at 0.10 μm. Except at the 0.1-μm gate length discussed above, these switching times were typically measured at a V_{dd} of 1.4–1.5 V, with a power consumption of ~0.14 mW per μm of gate width. For the 0.1-μm-gate-length ring oscillators, the shortest room-temperature delay was found to be 17.7 ps at V_{dd} = 1.3 V, with 0.12 mW of power consumption per 1 μm of gate width. Measurements of the inverter chains gave results which were consistent with those obtained from the ring oscillators.

Detailed circuit simulations (ASTAP) [30], in which the measured device characteristics were used as input, showed that the measured delay times were ~6 ps longer at LT, and ~7 ps longer at RT, than expected on the basis of device performance. The discrepancy was due to the high sheet resistivity of the $TiSi_2$. The resistivity increase with decreasing line width also resulted in the anomaly that the circuits which contained the 0.07-μm devices were actually the slowest. The results of the simulations, giving delay as a function of silicide resistivity, are shown in **Figure 12**. As can be seen, if the *RC* time constant associated with the gate resistance had not limited the switching performance, the 0.1-μm-gate-length ring oscillators might have reached a delay per stage of 7 ps. As indicated in the figure, in a horizontally fully scaled version of the circuits, fabricated, for instance, with shallow trenches thereby decreasing junction capacitance, delay per stage is expected to drop to about 5 ps.

As a final note, a few comments may be useful regarding the various possible trade-offs which pertain to the S/D junction edges in the case of transport far from

equilibrium. For the devices discussed, the gate overlap of the S/D was only ~10 nm per side. Such a short overlap is advantageous because it reduces the interelectrode capacitances. With a larger gate overlap, the transconductance of the devices would have been even higher (through S/D resistance reduction), but the delay time in the circuits slower. In dense circuits, where wiring capacitance is significant, it might be preferable to fabricate devices with a slightly larger gate-to-S/D overlap in order to gain in transconductance, even at the expense of some increase in gate capacitance. Such trade-offs occur at any gate length; however, at 0.1-μm dimensions they become more complicated because, as mentioned earlier, details of the transport that can safely be neglected for longer channels become significant at about 0.1 μm [8, 25].

Concluding remarks

The extendibility of silicon FET technology to the 0.1-μm-gate-length level has been experimentally investigated. In the course of the work, the best values to date have been obtained for transconductance and switching time. Overall, it appears that a low-temperature 0.1-μm-gate-length FET technology should be possible without abandoning mainline fabrication approaches. Although not apparent from the present work, the greatest future challenge appears to be in lithography. The resolution and alignment aspects of the electron-beam system which was used were excellent, but the system lacked adequate throughput capability. However, lithography is progressing on all fronts, from the more conventional approaches to X-ray systems, and to higher-throughput electron-beam systems. There is every reason to believe that the 0.1-μm regime will also be conquered. Selective formation of 0.1-μm-level features with adequate throughput is practically within reach already. We hope that our work provides added motivation to continue with FET miniaturization, even down to the 0.1-μm level.

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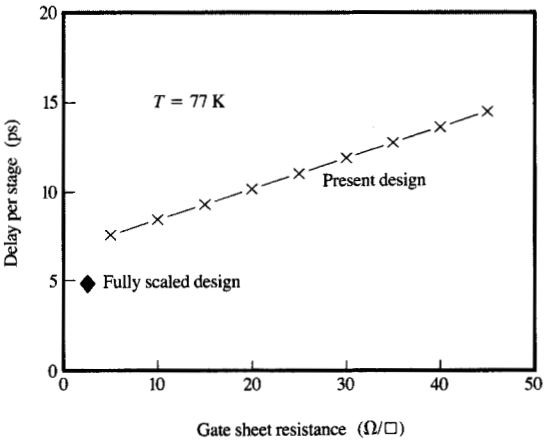

Figure 12

ASTAP simulation of the effects of $TiSi_2$ sheet resistance on the delay per stage, due to the *RC* time constant of the gates. The "fully scaled design" point assumes unchanged oxide thickness but reduced junction capacitance. The size and layout of the simulated ring oscillator duplicated those of the fabricated circuits.

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